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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TANG, KUO LIANG J	

ART UNIT	PAPER NUMBER
2122	

DATE MAILED: 12/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/998,848	OGAMI, KENNETH Y.	
	Examiner	Art Unit	
	Kuo-Liang J Tang	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the application filed on 11/15/2001.

The priority date for this application is 11/15/2001.

Claims 1-35 are pending and have been examined.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-35 are rejected under 35 U.S.C. 102(b) as being anticipated by Bindra, "Programmable SoC Delivers A New Level Of System Flexibility". Electronic Design, November 6, 2000 and Cypress MicroSystems and which incorporated "PSoC Designer: Integrated Development Environment, Getting Started 25-Minute Tutorial, Revision 1.0", Cypress MicroSystems, Inc., CMS10006A, July 3, 2001 (hereinafter **PsocTutor**), "PSoC Technology Complete Changes 8-Bit MCU System Design",Cypress MicroSystem, Inc. 02/19/2001 (hereinafter **PsocTech**), Cypress MicroSystem, Inc, "Cypress Customer Forums", 2/21/2001 (hereinafter **PsocForum**) and "PsoC Designer: Integrated Development Environment User Guide", Cypress MicroSystem, Inc., rev 1.18, 9/8/2003 (hereinafter **PsocIde**).

It should be noted that **PsocTutor**, **PsocTech**, **PsocForum** and **PsocIde** are incorporated and/or as per MPEP 2131.01, applied, to:

(A) Prove the primary reference contains an "enabled disclosure;"

(B) Explain the meaning of a term used in the primary reference; or

(C) Show that a characteristic not disclosed in the reference is inherent.

As Per Claim 1, Bindra teaches System-on-a-chip (SoC) solutions have primarily been digitally intensive, comprised of a micro-controller/DSP core, memory, logic, interfaces, and other similar functions on the same die. In terms of flexibility and reconfigurability, these CPU-centric designs have been dictated by the programmability of the on-chip processor and memory (page 1, 1st para.). PSoC Designer software product comprises three subsystems. These include a device editor, an application editor, and a debugger. In the device editor mode, user modules are selected, pins are assigned, and register mappings are established (page 2, 2nd para,). And the PSoC Designer is an integral part of the Windows-based development process. Its device editor employs a graphical interface to connect user modules, which are next mapped onto the SoCblocs on-chip. Finally, the user selects the pin assignments (E.g. see Bindra, page 11, Fig 4). In that Bindra discloses features of the PsoC Designer product for configuring a microcontroller that covering the steps of:

"displaying a collection of virtual blocks in a design system with each virtual block in said collection corresponding to a programmable block in said microcontroller" (E.g. see Bindra, page 11, Fig 4);

"selecting a user module defining a function" (E.g. see Bindra, page 11, Fig 4 and associated text and further see **PsocTutor**, page 8, Figure 5 User Module Selection of the PsoC Designer product and associated text);

"assigning a virtual block taken from said collection to said user module" (E.g. see Bindra, page 11, Fig 4 and associated text and further see **PsocTutor**, page 9, Figure 6 and associated text); and

"automatically constructing a source code table file comprising configuration information for a programmable block of said microcontroller corresponding to said virtual block wherein said configuration information is used to cause said programmable block to implement said function" (E.g. see Bindra, page 11, Fig 4 and associated text and further see **PsocTutor**, pages 14-17).

As Per claim 2, the rejection of claim 1 is incorporated and further Bindra teaches:

"wherein said function comprises a pulse width modulator" (E.g. see Bindra, page 2, line 36, pulse-width modulators (PWMs)).

As Per claim 3, the rejection of claim 1 is incorporated and further Bindra teaches:

"wherein said function comprises a timer" (E.g. see Bindra, page 3, line 9).

As Per claim 4, the rejection of claim 1 is incorporated and further Bindra teaches:

"wherein said function comprises an analog-to-digital converter" (E.g. see Bindra, page 2, line 25).

As Per claim 5, the rejection of claim 1 is incorporated and further Bindra teaches:

"wherein said function comprises a digital-to-analog converter" (E.g. see Bindra, page 2, line 35).

As Per claim 6, the rejection of claim 1 is incorporated and further Bindra teaches:

"wherein said function comprises a counter" (E.g. see Bindra, page 2, line 36).

As Per claim 7, the rejection of claim 1 is incorporated and further Bindra teaches:

"wherein said function comprises a signal amplifier" (E.g. see Bindra, page 2, line 36).

As Per claim 8, the rejection of claim 1 is incorporated and further Bindra teaches:

"wherein said function provides serial communication" (E.g. see Bindra, page 2, lines 27-28, 33, and page 3, lines 13-14).

As Per claim 9, the rejection of claim 1 is incorporated and further Bindra teaches:

"wherein said collection is displayed as a two dimensional array of programmable analog virtual blocks and programmable digital virtual blocks". (E.g. see Bindra, page 11, Fig. 4 and associated text).

As Per claim 10, the rejection of claim 1 is incorporated and further Bindra includes **PsocTutor** teaches:

"wherein said assigning further comprises assigning a second virtual block to said user module" (E.g. see Bindra, page 11, Fig 4 and associated text and further see **PsocTutor**, page 9, Figure 6 and associated text).

As Per claim 11, the rejection of claim 1 is incorporated and further Bindra includes **PsocTutor** teaches:

"wherein said code table file is an assembly (E.g. see Bindra, page 11, Fig 4 and associated text and PsocTech, page 13, lines 1-5) code table file and further comprises: a symbolic name for a register address in said programmable block" (E.g. see Bindra, page 11, Fig 4 and associated text and further see **PsocTutor**, pages 15-16, Figures 14-15).

As Per claim 12, the rejection of claim 11 is incorporated and further Bindra includes **PsocTutor** and **PsocIde** teaches:

"wherein said symbolic name is derived from said function" (E.g. see Bindra, page 11, Fig 4 and associated text and further see **PsocTutor**, pages 15-16, Figures 14-15 and **PsocIde**, pages 98-106 and pages 115-116, Section 6.5.1).

As Per claim 13, Bindra includes **PsocTutor** and **PsocIde** teaches a method of configuring a microcontroller having a programmable block, said method comprising:

"selecting a user module defining a circuit design" (E.g. see Bindra, page 11, Fig 4 and associated text and further see **PsocTutor**, page 8, Figure 5 & see page 3 and associated text);

"assigning a virtual block in a design system where said virtual block corresponds to said programmable block" (E.g. see Bindra, page 11, Fig 4 and associated text and further see **PsocTutor**, page 9, Figure 6 and associated text); and

"automatically constructing an assembly code file holding configuration information for said programmable block to implement said circuit design" (E.g. see Bindra, page 11, Fig 4 and associated text and further see **PsocTutor**, pages 14-17 and **PsocIde**, pages 98-106 and pages 115-116, Section 6.5.1).

As Per claim 14, the rejection of claim 13 is incorporated and further Bindra includes **PsocTutor** and **PsocIde** teaches:

"computing a register address for a register within said programmable block;

determining a symbolic name for said register address; and

placing said symbolic name into said assembly code file" (E.g. see Bindra, page 11, Fig 4 and associated text and further see **PsocTutor**, pages 14-17 and **PsocIde**, pages 98-106).

As Per claim 15, the rejection of claim 14 is incorporated and further Bindra includes **PsocTutor** and **PsocIde** teaches:

"substituting said symbolic name for a generic name in a template file" (E.g. see Bindra, page 11, Fig 4 and associated text and further see **PsocTutor**, pages 14-17 and **PsocIde**, page 105, line 22, "boot.tpl" and page 121, lines 20-22)

As Per Claim 16, the rejection of claim 13 is incorporated and further Bindra includes **PsocTutor** and **PsocIde** teaches:

"determining a symbolic name; computing a register address for a register within said programmable block; assigning said symbolic name to said register address; and placing said symbolic name into said assembly code file" (E.g. see Bindra, page 11, Fig 4 and associated text and further see **PsocTutor**, pages 14-17 and **PsocIde**, pages 98-106).

As Per claim 17, Bindra includes **PsocTutor** and **PsocIde** teaches a method of configuring a microcontroller having a programmable block, said method comprising:

"selecting a user module defining a function" (E.g. see Bindra, page 11, Fig 4 and associated text and further see **PsocTutor**, page 8, Figure 5 & page 3 and associated text);

"assigning a virtual block in a design system where said virtual block corresponds to said programmable block" (E.g. see Bindra, page 11, Fig 4 and associated text and further see **PsocTutor**, page 9, Figure 6 and associated text); and

"automatically constructing an assembly code file with personalization information specifying said programmable block as performing said function" (E.g. see Bindra, page 11, Fig 4 and associated text and further see **PsocTutor**, pages 14-17 and **PsocIde**, pages 98-106 and pages 115-116, Section 6.5.1).

As per Claims 18-20, the rejection of claim 17 are incorporated and are rejected under the same reason set forth in connection of the rejection of claims 14-16 respectfully.

As Per claim 21, Bindra includes **PsocTutor** and **PsocIde** teaches a method of configuring a microcontroller having a programmable block, said method comprising:

"selecting a user module defining a function having a control parameter" (E.g. see Bindra, page 11, Fig 4 and associated text and further see **PsocTutor**, page 8, Figure 5 and associated text);

"assigning a virtual block in a design system where said virtual block corresponds to said programmable block" (E.g. see Bindra, page 11, Fig 4 and associated text and further see **PsocTutor**, page 9, Figure 6 and associated text); and

"constructing an assembly code file operating said control parameter within said programmable block" (E.g. see Bindra, page 11, Fig 4 and associated text and further see **PsocTutor**, pages 14-17 and **PsocIde**, pages 98-106 and pages 115-116, Section 6.5.1).

As per Claims 22-24, the rejection of claim 21 are incorporated and are rejected under the same reason set forth in connection of the rejection of claims 14-16 respectfully.

As Per claim 25, Bindra includes **PsocTutor** and **PsocIde** teaches a method of configuring a microcontroller having a programmable block, said method comprising:

"selecting a user module defining a function having a control parameter" (E.g. see Bindra, page 11, Fig 4 and associated text and further see **PsocTutor**, page 8, Figure 5 & page 3 and associated text);

"assigning a virtual block in a design system where said virtual block corresponds to said programmable block" (E.g. see Bindra, page 11, Fig 4 and associated text and further see **PsocTutor**, page 9, Figure 6 and associated text);

"constructing an assembly code routine using said control parameter" (E.g. see Bindra, page 11, Fig 4 and associated text and further see **PsocTutor**, pages 14-17 and **PsocIde**, pages 98-106 and and **PsocIde**, pages 115-116, Section 6.5.1); and

"constructing a header file referencing said assembly code routine" (E.g. see Bindra, page 11, Fig 4 and associated text and further see **PsocTutor**, pages 14-17 and **PsocIde**, pages 98-106 and pages 115-116, Section 6.5.1, page 101, Figure 57 and associated text).

As Per Claim 26, is the system claim corresponding to the method claim 1 and is rejected under the same reason set forth in connection of the rejection of claim 1.

As per Claims 27-30, the rejection of claim 26 are incorporated and are rejected under the same reason set forth in connection of the rejection of claims 9-12 respectfully.

As Per claim 31, Bindra includes **PsocTutor** and **PsocIde** teaches a computer implemented method of generating program information for a programmable electronic device comprising:

"a) selecting a user module, wherein said user module is defined by a first data structure" (E.g. see Bindra, page 11, Fig 4 and associated text and further see **PsocTutor**, page 8, Figure 5 & page 3 and associated text);

"b) placing said user module within a hardware resource of said programmable electronic device, wherein said hardware resource is defined by a second data structure" (E.g. see Bindra,

page 11, Fig 4 and associated text and further see **PsocTutor**, page 9, Figure 6 and associated text);

"c) using said first and second data structures lo automatically generate first source code for realizing said user module within said hardware resource" (E.g. see Bindra, page 11, Fig 4 and associated text and further see **PsocTutor**, pages 14-17 and **PsocIde**, pages 98-106 and pages 115-116, Section 6.5.1, page 101, Figure 57 and associated text); and

"d) saving said first source code in a computer file" (E.g. see Bindra, page 11, Fig 4 and associated text and further see **PsocTutor**, pages 14-17 and **PsocIde**, page 79, line 7 and page 138, line 11).

As Per claim 32, the rejection of claim 31 is incorporated and further Bindra includes **PsocTutor** and **PsocIde** teaches:

"e) selecting parameter values that define the behavior of said user module such that it operates in a prescribed manner" (E.g. see Bindra, page 11, Fig 4 and associated text and further see **PsocIde**, page 76, Figure 45 and associated text);

"f) automatically generating second source code, based on said parameter values, for causing said user module of said hardware resource to behave in said prescribed manner" (E.g. see Bindra, page 11, Fig 4 and associated text and further see **PsocIde**, pages 98-106, Section 5.8); and

"g) saving said second source code in a computer file" (E.g. see Bindra, page 11, Fig 4 and associated text and further see **PsocTutor**, pages 14-17 and **PsocIde**, page 79, line 7 and page 138, line 11).

As Per claim 33, the rejection of claim 32 is incorporated and further Bindra includes **PsocIde** teaches:

"using said first and second source code to program said programmable electronic device" (E.g. see Bindra, page 11, Fig 4 and associated text and further see **PsocIde**, pages 98-106, Section 5.8).

As Per claim 34, the rejection of claim 33 is incorporated and further Bindra includes **PsocIde** teaches:

"wherein said programmable electronic device is a microcontroller" (E.g. see Bindra, page 11, Fig 4 and associated text and further see **PsocIde**, page 96, line 22, MCU).

As Per claim 35, the rejection of claim 31 is incorporated and further Bindra includes **PsocTutor** and **PsocIde** teaches:

"wherein said a) and said e) are performed using a graphical user interface" (E.g. see Bindra, page 11, Fig 4 and associated text and further see **PsocTutor**, page 8, Figure 5 and associated text and **PsocIde**, page 76, Figure 45 and associated text).

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kuo-Liang J Tang whose telephone number is (571) 272-3705. The examiner can normally be reached on 8:30AM - 7:00PM (Monday – Thursday).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kuo-Liang J. Tang

Software Engineer Patent Examiner

TUAN DAM
SUPERVISORY PATENT EXAMINER